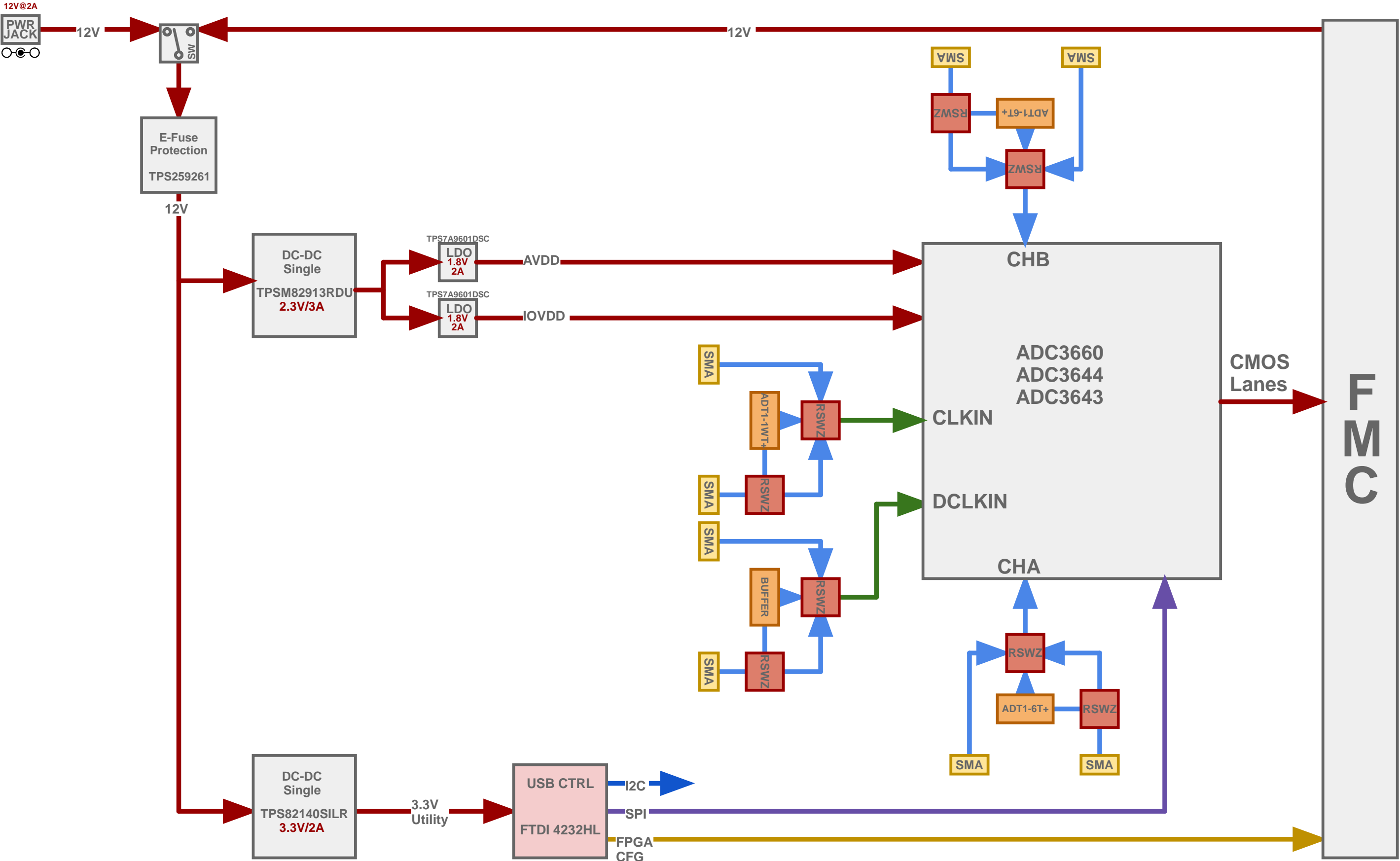


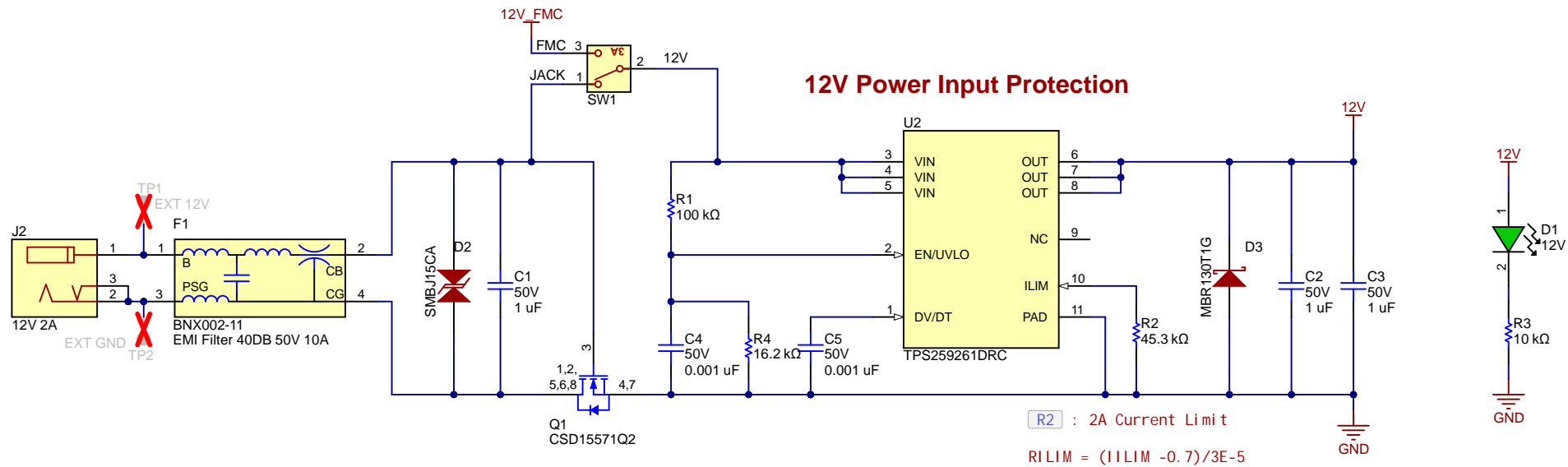
Block Diagram



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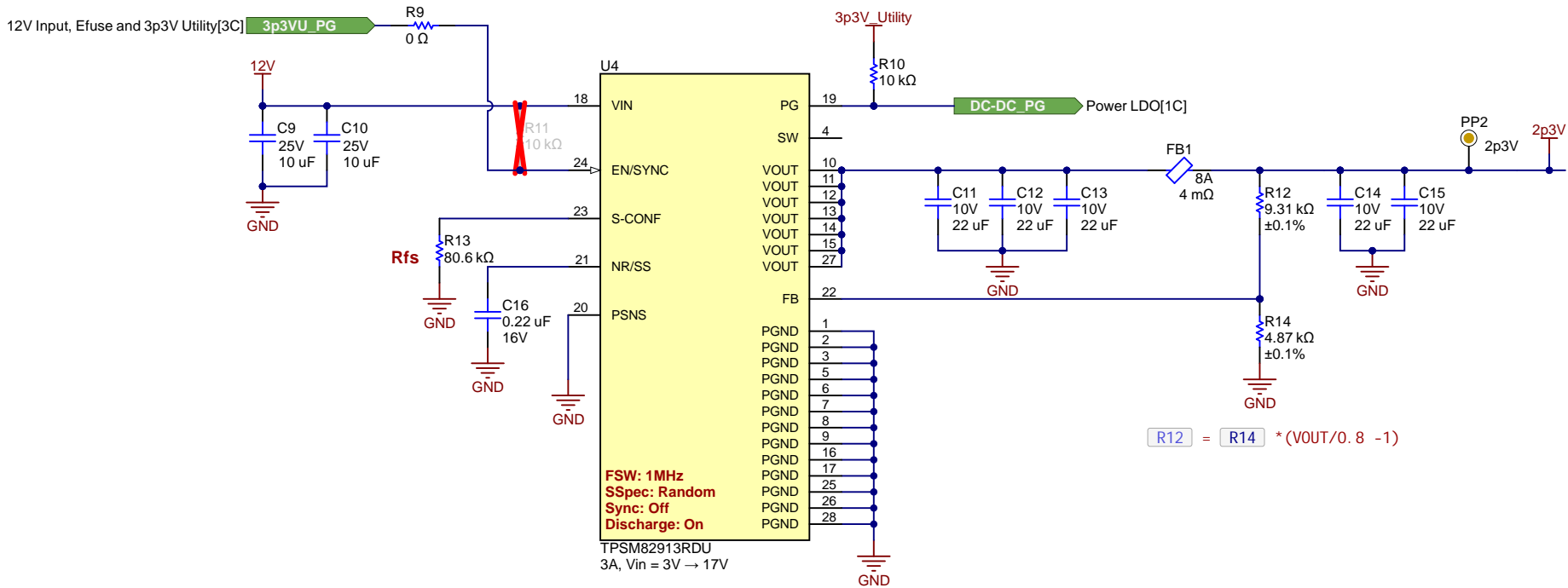
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| Orderable: ChangeMe in variant | Designed for: Public Release | Mod. Date: 8/27/2025 |
| TID #: N/A | Project Title: ADC3644EVM | |
| Number: DC104 | Rev: G2 | Sheet Title: Block Diagram |
| SVN Rev: 4d8f6644f88f576e517212000035654fdd63703 (ADC3660) | | Sheet: 1 of 15 |
| Drawn By: GBR | File: Block Diagram.SchDoc | Size: B |
| Engineer: GBR | Contact: http://www.ti.com/support | |

12V Input & 3.3V Utility



| | | |
|--|--|---|
| Orderable: ChangeMe in variant | Designed for: Public Release | Mod. Date: 8/27/2025 |
| TID #: N/A | Project Title: ADC3644EVM | |
| Number: DC104 | Rev: G2 | Sheet Title: 12V Input & 3.3V Utility |
| SVN Rev: c5e7066f3c60874fd8f4c346880f30e5d1903 | ADC3660 | Sheet: 2 of 15 |
| Drawn By: GBR | File: 12V Input, Efuse and 3p3V Utility.SchDoc | Size: B |
| Engineer: GBR | Contact: http://www.ti.com/support | |

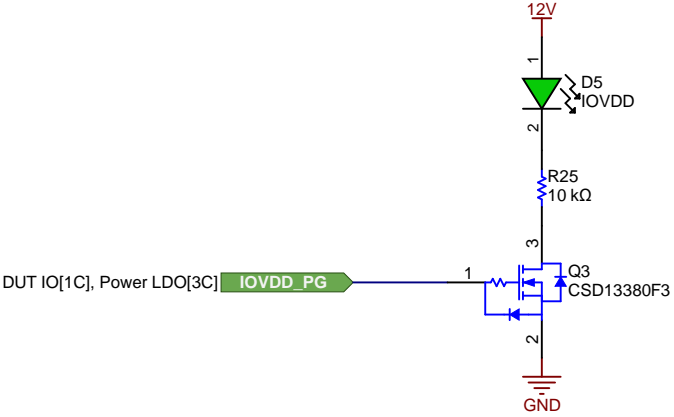
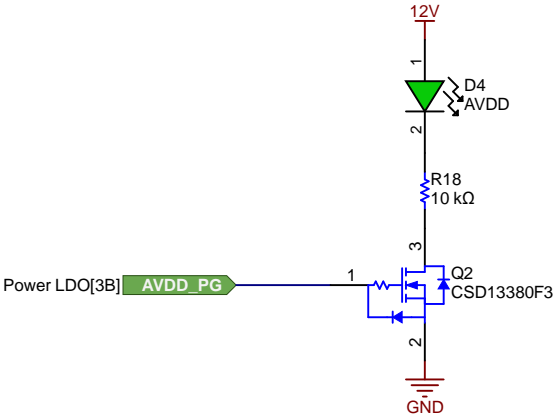
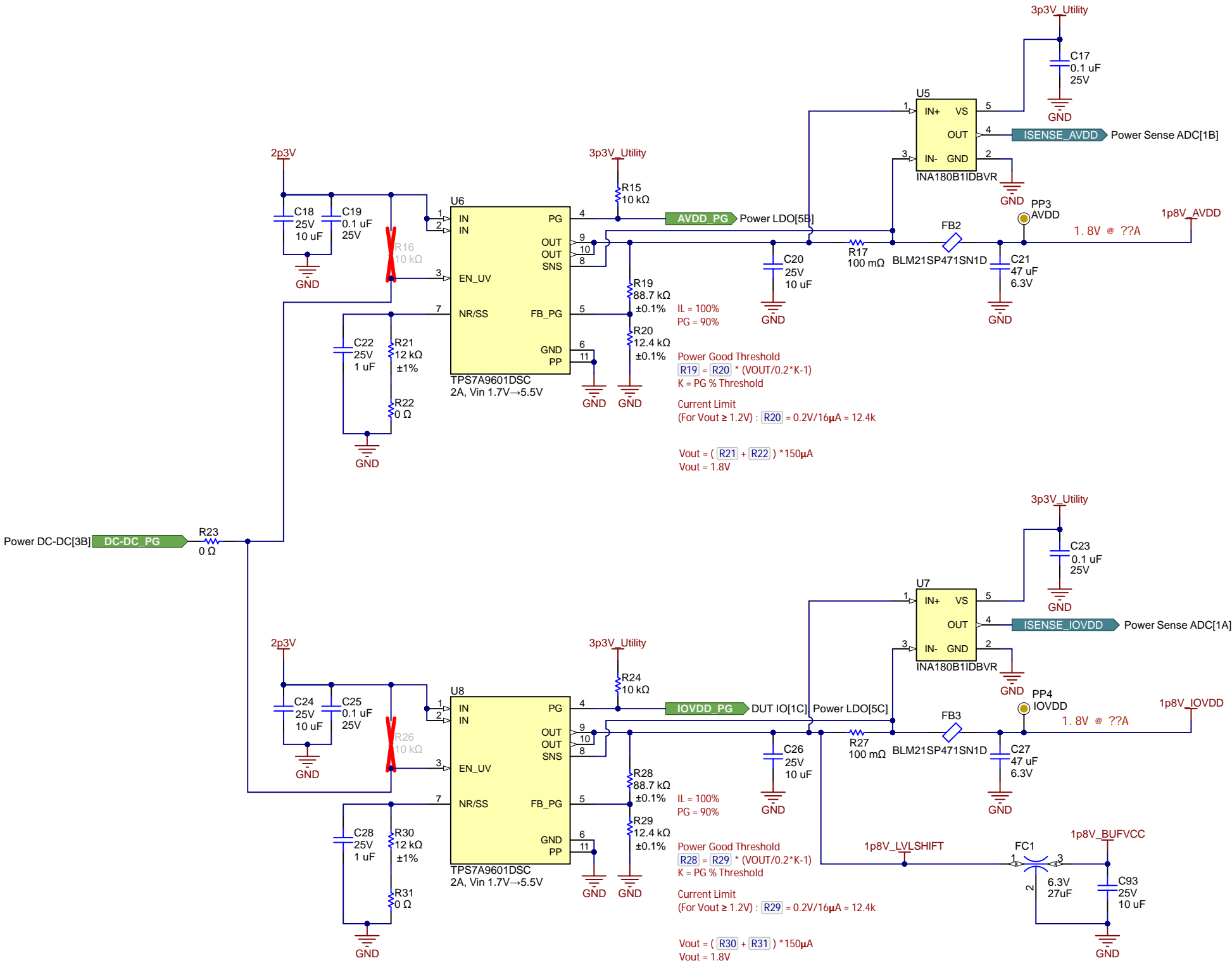
DC/DC regulator



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|--|--|--|
| Orderable: ChangeMe in variant | Designed for: Public Release | Mod. Date: 8/27/2025 |
| TID #: N/A | Project Title: ADC3644EVM | |
| Number: DC104 | Rev: G2 | Sheet Title: DC/DC regulator |
| SVN Rev: c5e7066f3c60874fd8f4c346880f30e5d4903 | File: Power DC-DC.SchDoc | Size: B |
| Drawn By: GBR | Contact: http://www.ti.com/support | |

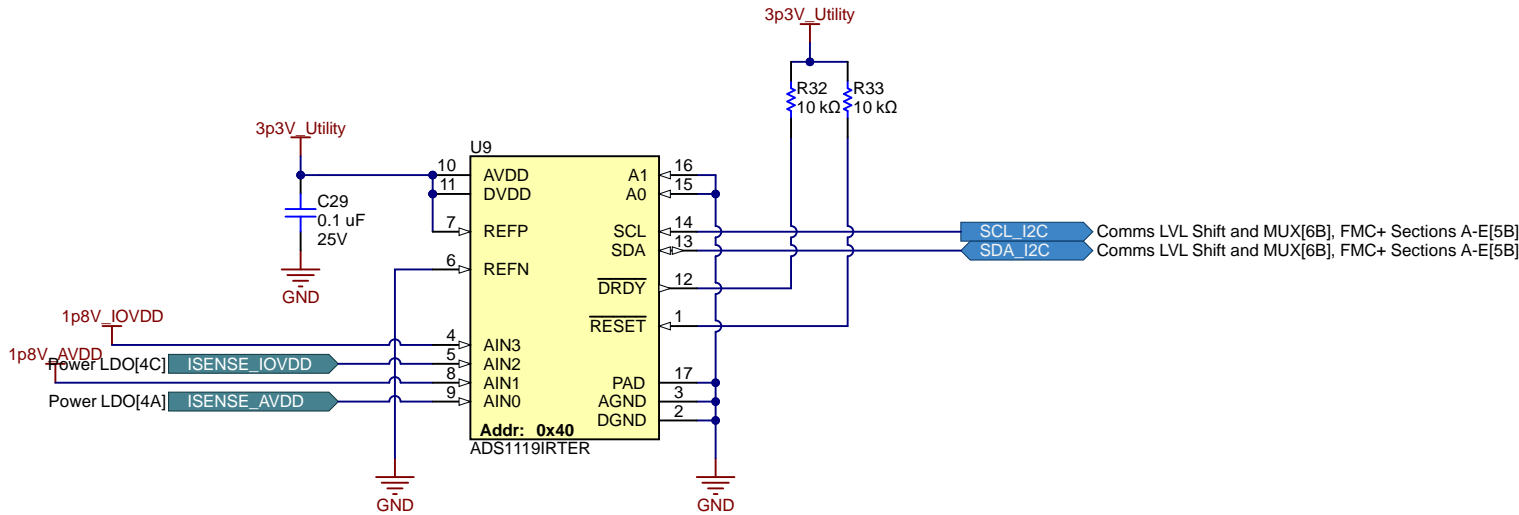
LDOs



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| | | |
|--|--|--|
| Orderable: ChangeMe in variant | Designed for: Public Release | Mod. Date: 8/27/2025 |
| TID #: N/A | Project Title: ADC3644EVM | |
| Number: DC104 | Rev: G2 | Sheet Title: LDOs |
| SVN Rev: c5e7066f3c60874fd8f4c346880f30e5d1903 | File: Power LDO.SchDoc | Sheet: 4 of 15 |
| Drawn By: GBR | Contact: http://www.ti.com/support | Size: B |

Sense ADC

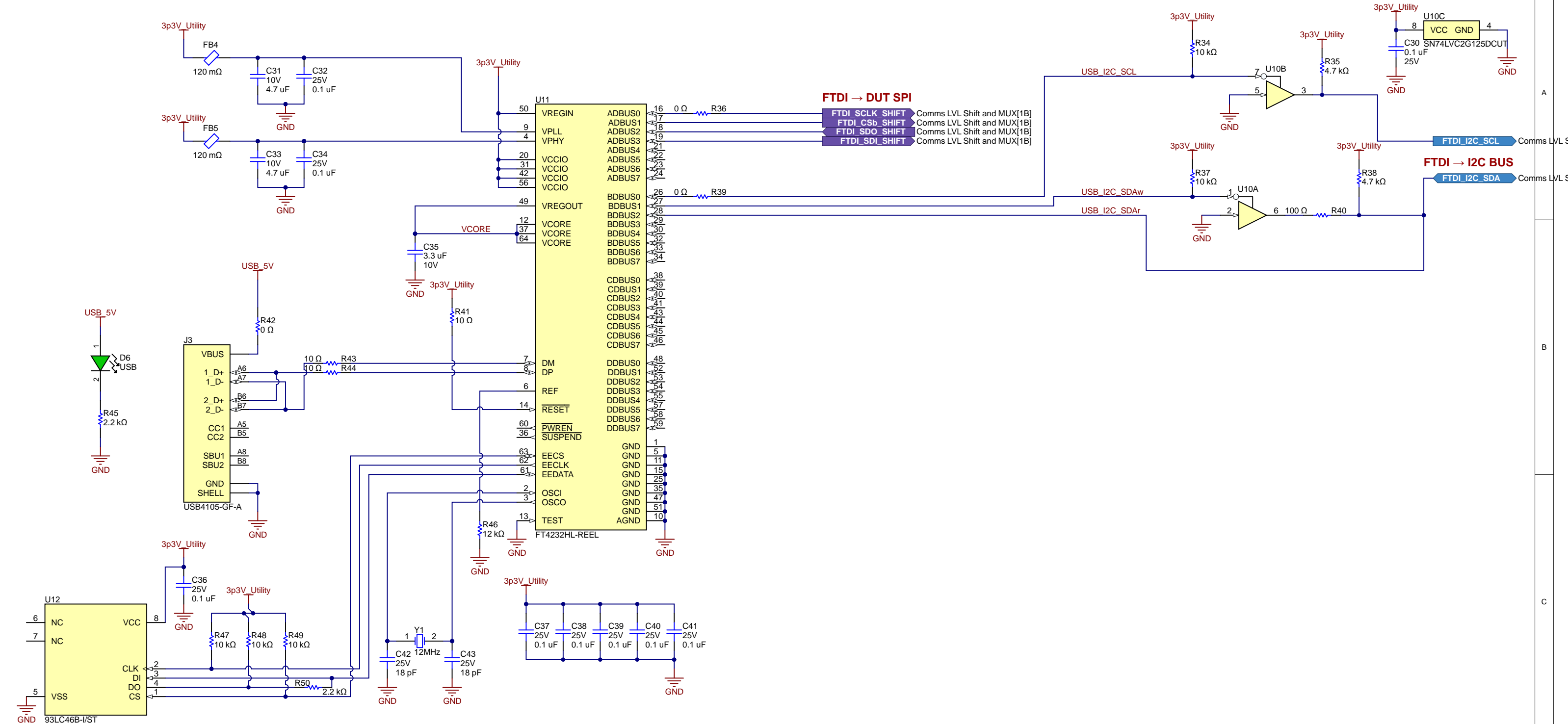


| ADS1119RTE Addresses | | |
|----------------------|------|------|
| A0 | A1 | Addr |
| GND | GND | 0x40 |
| GND | DVDD | 0x41 |
| GND | SDA | 0x42 |
| GND | SCL | 0x43 |
| DVDD | GND | 0x44 |
| DVDD | DVDD | 0x45 |
| DVDD | SDA | 0x46 |
| DVDD | SCL | 0x47 |
| SDA | GND | 0x48 |
| SDA | DVDD | 0x49 |
| SDA | SDA | 0x4A |
| SDA | SCL | 0x4B |
| SCL | GND | 0x4C |
| SCL | DVDD | 0x4D |
| SCL | SDA | 0x4E |
| SCL | SCL | 0x4F |

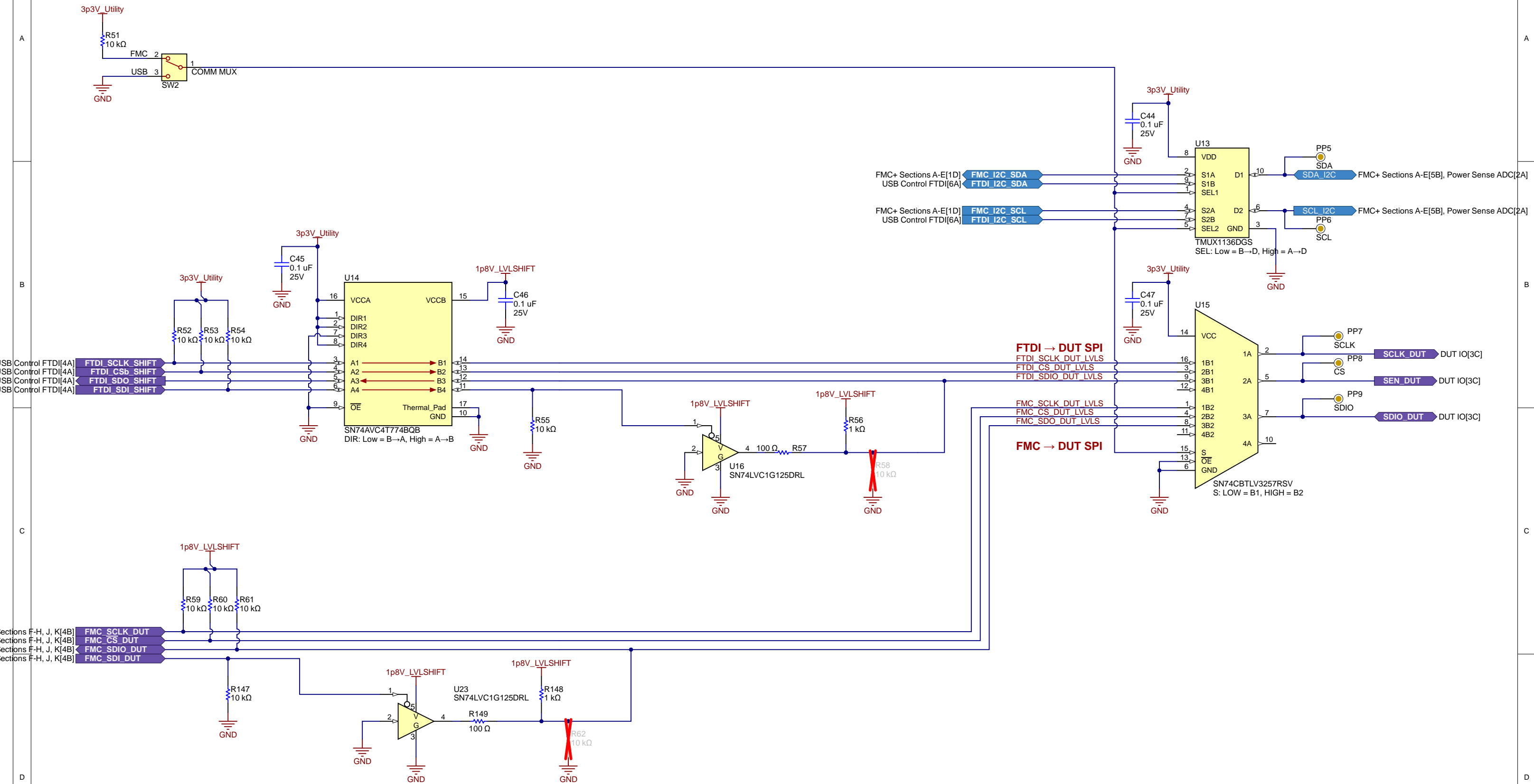
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| | | | |
|---|--|--|----------------------|
| Orderable: ChangeMe in variant | | Designed for: Public Release | Mod. Date: 8/27/2025 |
| TID #: N/A | Project Title: ADC3644EVM | | |
| Number: DC104 | Rev: G2 | Sheet Title: Sense ADC | |
| SVN Rev: c5e7066f3c60874fd8f4c346880f30e5d19003 | ADC3660 (ADC3660) | | Sheet: 5 of 15 |
| Drawn By: GBR | File: Power Sense ADC.SchDoc | | Size: B |
| Engineer: GBR | Contact: http://www.ti.com/support | | |

FTDI Control



Comms Lvl Shift & Mux



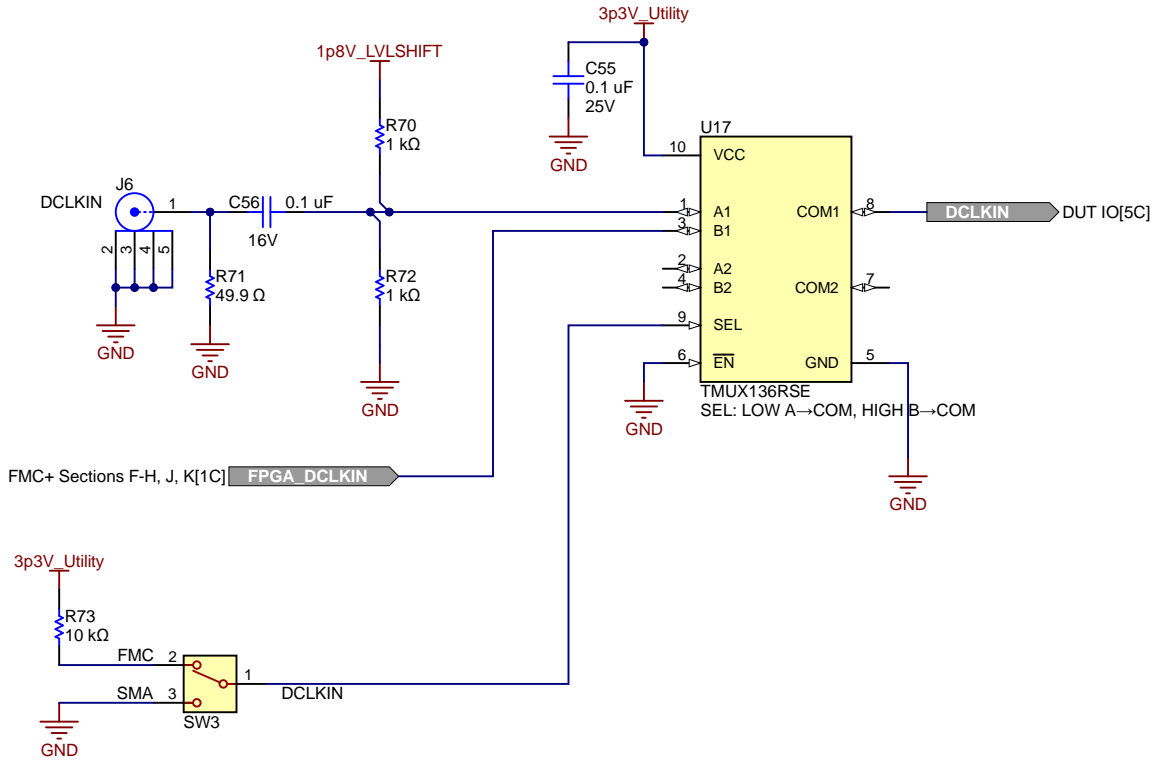
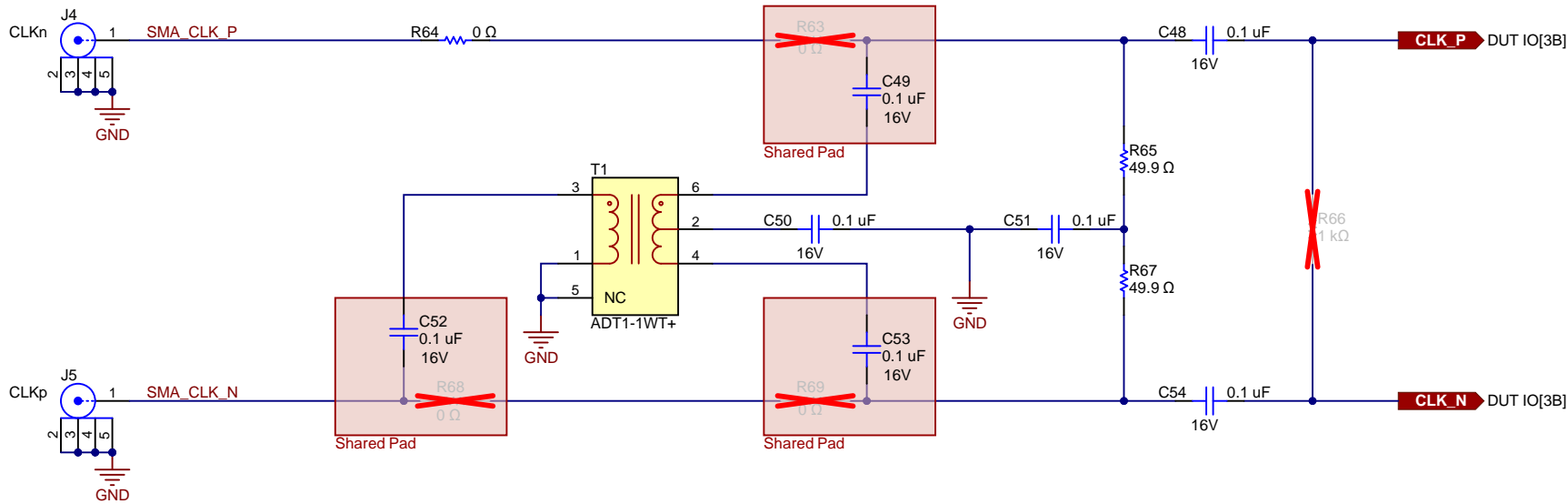
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|--|--|--|---|
| Orderable: ChangeMe in variant | Designed for: Public Release | Mod. Date: 8/27/2025 |  TEXAS INSTRUMENTS http://www.ti.com © Texas Instruments 2025 |
| TID #: N/A | Project Title: ADC3644EVM | | |
| Number: DC104 | Rev: G2 | Sheet Title: Comms Lvl Shift & Mux | |
| SVN Rev: d3304445bfb3aafcd1595332474a509e5f102 | | Sheet: 7 of 15 | |
| Drawn By: | File: Comms LVL Shift and MUX.SchDoc | Size: B | |
| Engineer: GBR | Contact: http://www.ti.com/support | | |

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CLK & DCLKIN

CLK

DCLKIN

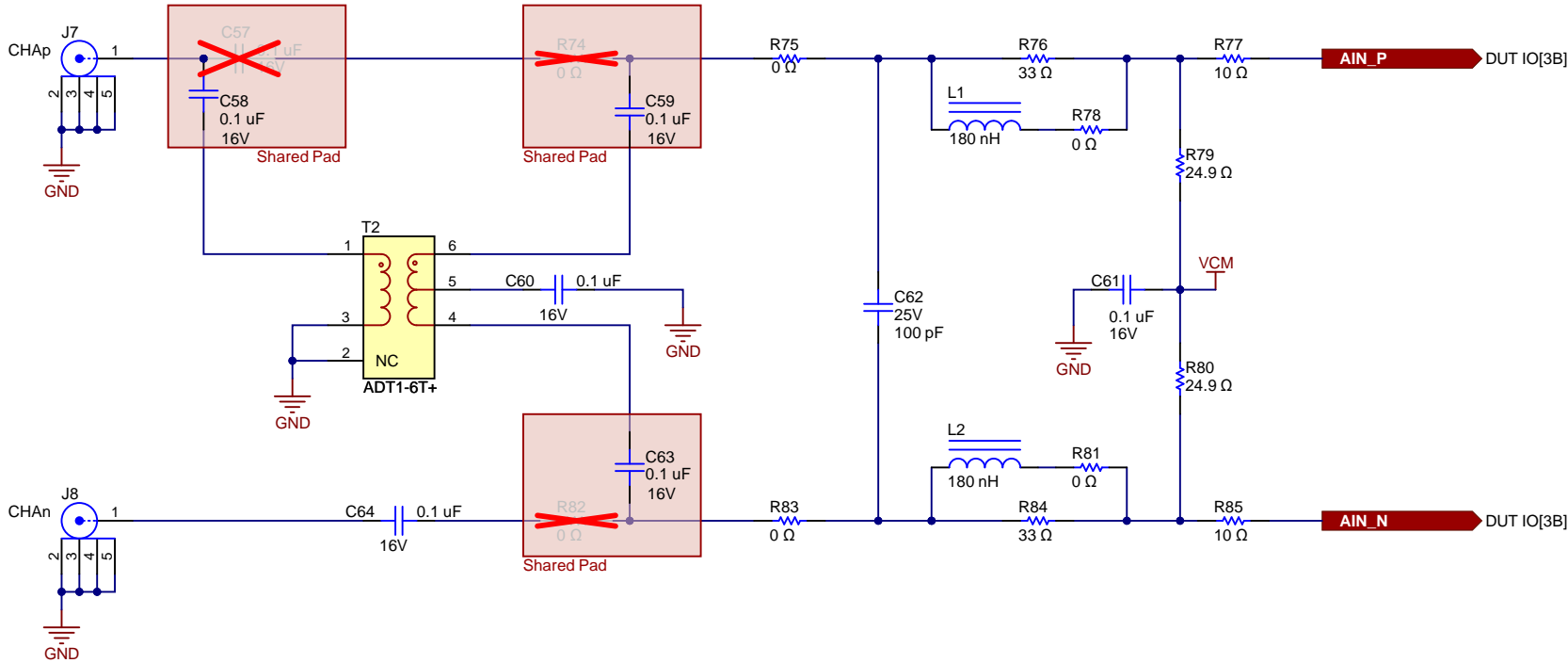


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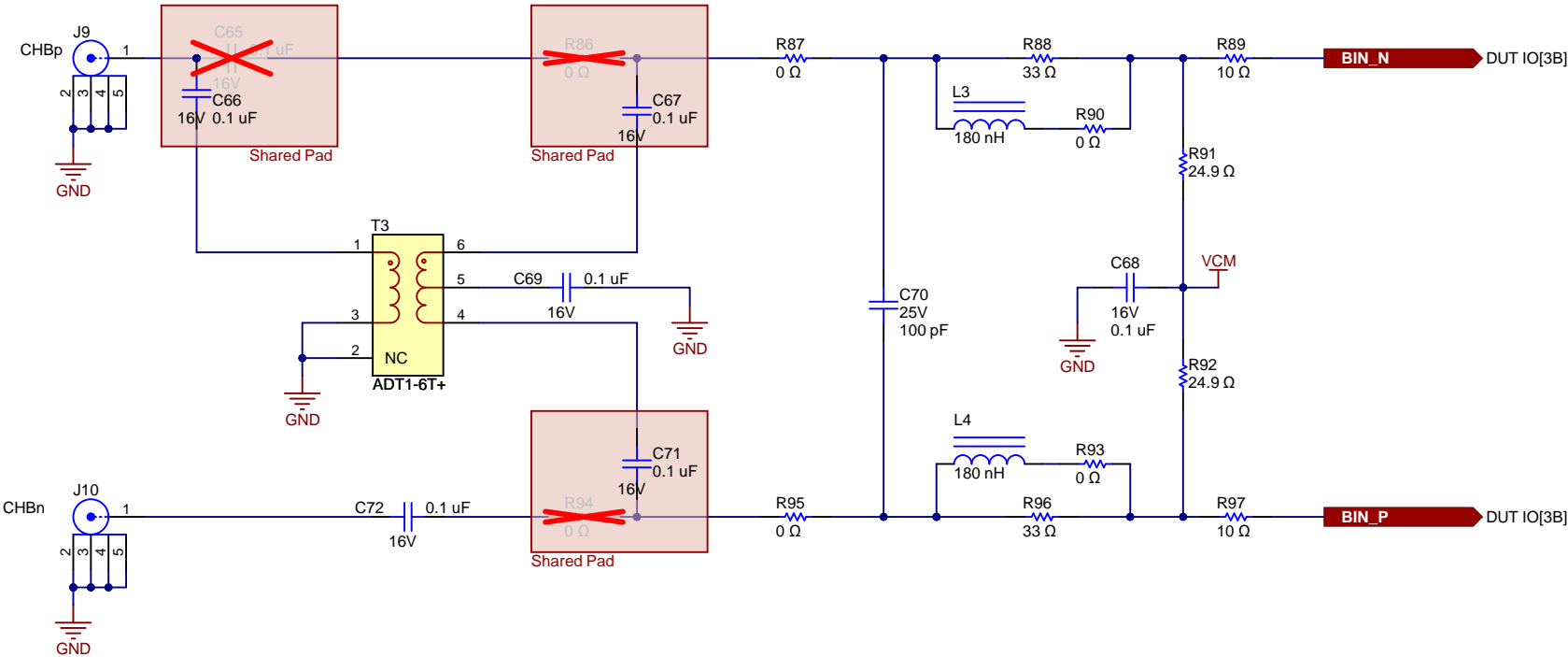
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| Number: DC104 | Rev: G2 | Sheet Title: CLK & DCLKIN |
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ADC Inputs

CH A



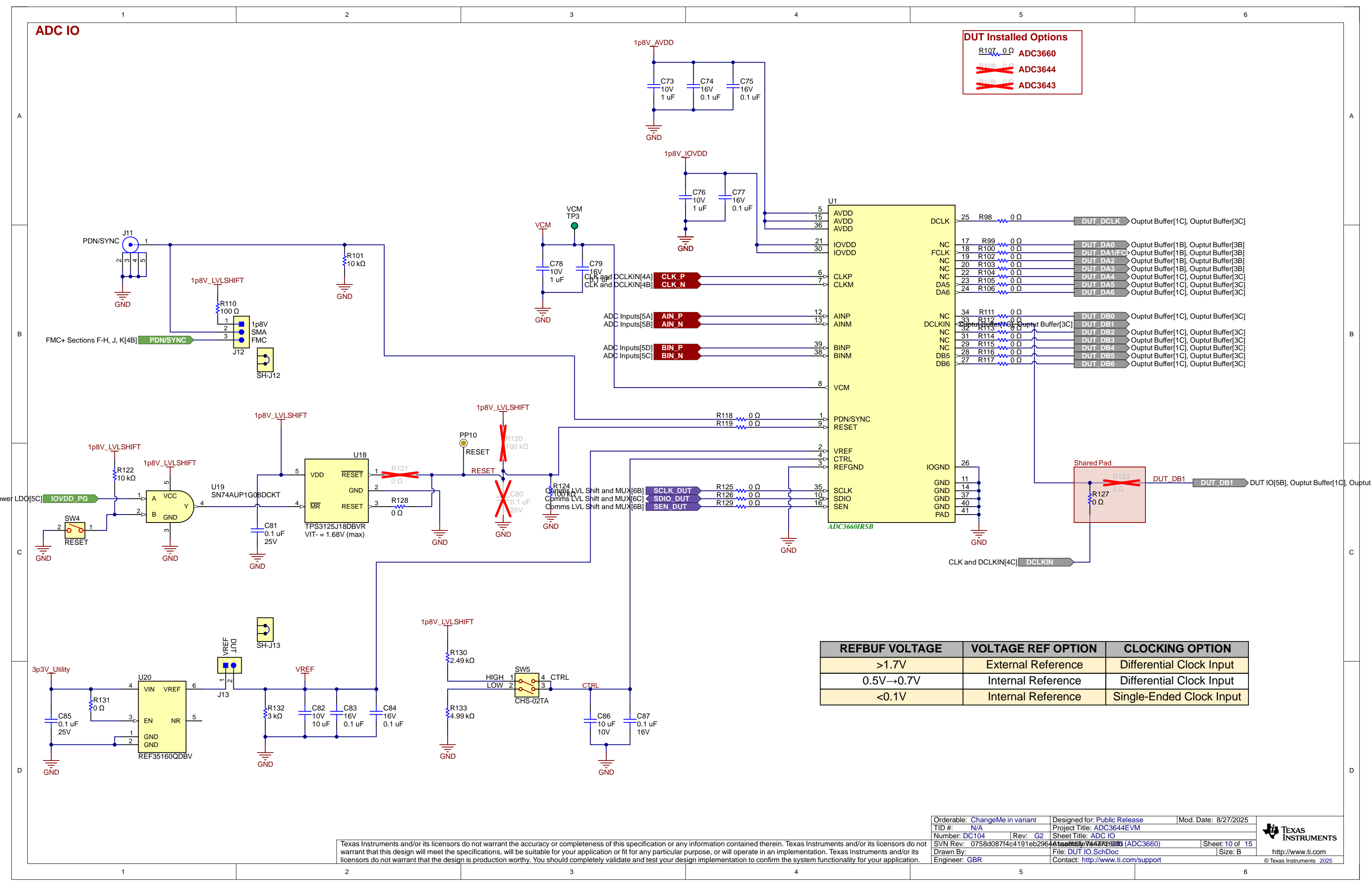
CH B



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| | | |
|---|--|---|
| Orderable: ChangeMe in variant | Designed for: Public Release | Mod. Date: 8/27/2025 |
| TID #: N/A | Project Title: ADC3644EVM | |
| Number: DC104 | Rev: G2 | Sheet Title: ADC Inputs |
| SVN Rev: 8c8b4ccc1816adc836182b2c2356324ee008 | File: ADC Inputs.SchDoc | Sheet: 9 of 15 |
| Drawn By: GBR | Contact: http://www.ti.com/support | Size: B |

ADC IO



| REFBUF VOLTAGE | VOLTAGE REF OPTION | CLOCKING OPTION |
|----------------|--------------------|--------------------------|
| >1.7V | External Reference | Differential Clock Input |
| 0.5V→0.7V | Internal Reference | Differential Clock Input |
| <0.1V | Internal Reference | Single-Ended Clock Input |

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|--|--|-------------------------------------|
| Orderable: ChangeMe in variant | Designed for: Public Release | Mod. Date: 8/27/2025 |
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| Number: DC104 | Rev: G2 | Sheet Title: ADC IO |
| SVN Rev: 0758d087f4c4191eb2964474722003 | Assembled by: ADC3660 | Sheet: 10 of 15 |
| Drawn By: GBR | File: DUT IO.SchDoc | Size: B |
| Engineer: GBR | Contact: http://www.ti.com/support | |

FMC+ Section Rows A - E

A

B

C

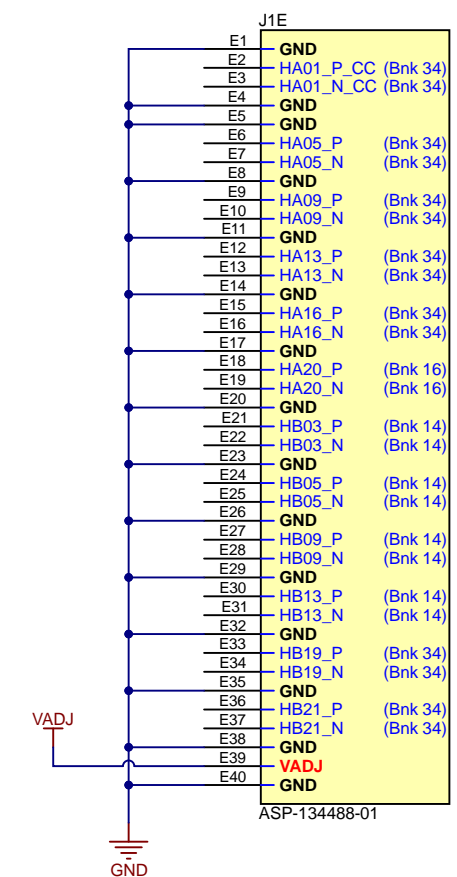
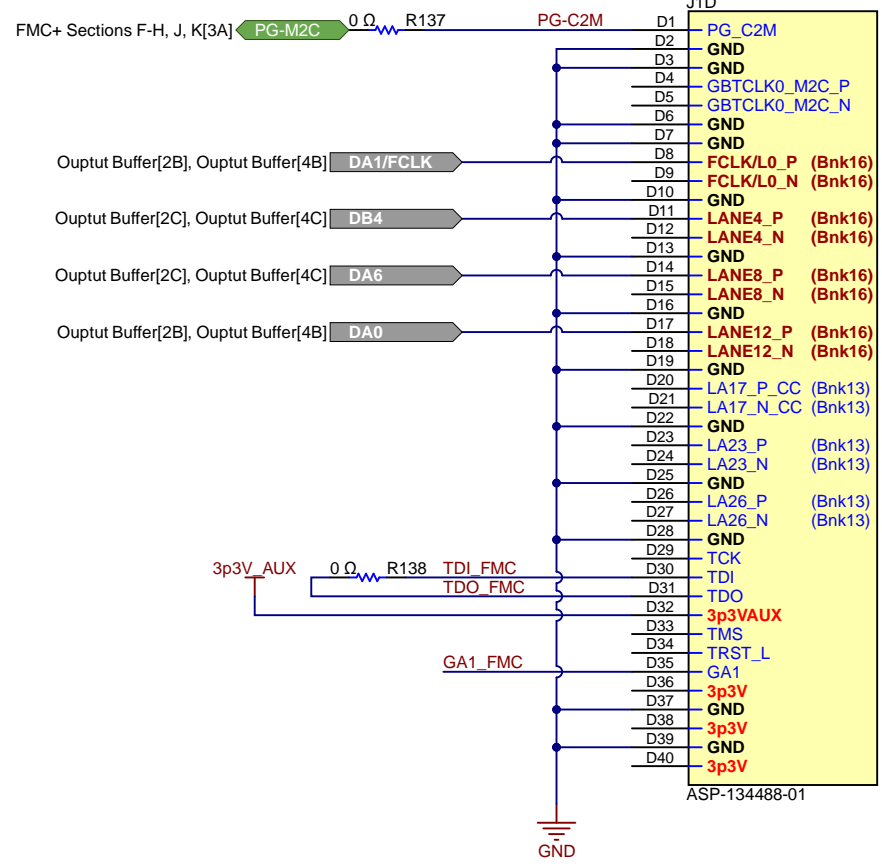
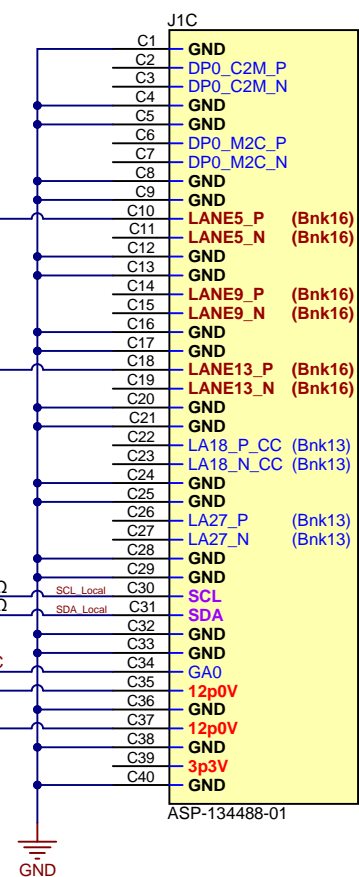
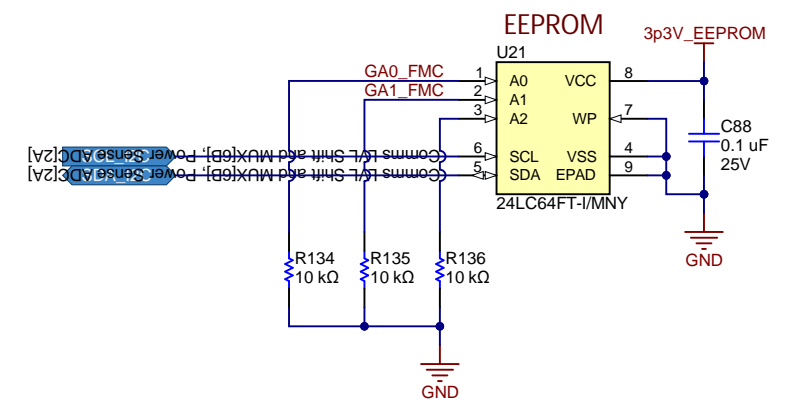
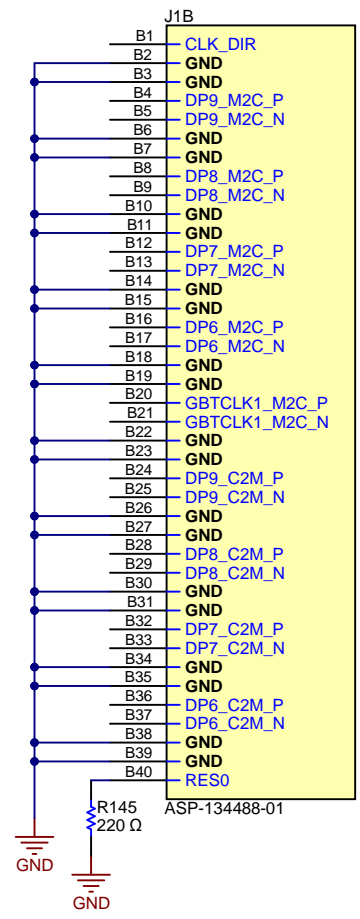
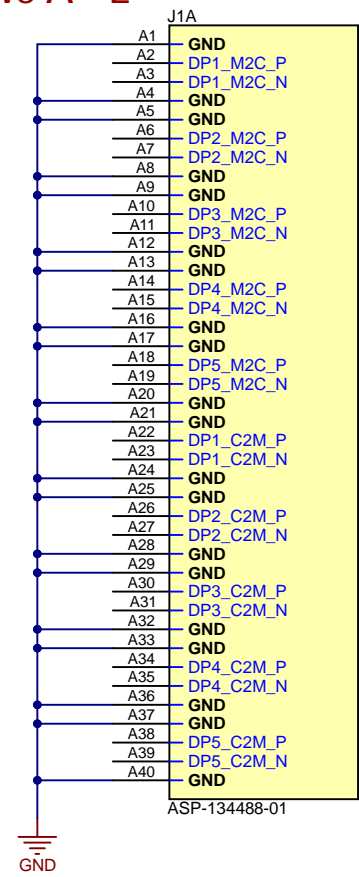
D

A

B

C

D



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|--|------------------------------------|--------------------------------------|
| Orderable: ChangeMe in variant | Designed for: Public Release | Mod. Date: 8/27/2025 |
| TID #: N/A | Project Title: ADC3644EVM | |
| Number: DC104 | Rev: G2 | Sheet Title: FMC+ Section Rows A - E |
| SVN Rev: c5e7066f3c60874fd8f4c346880f30e5d4903 | File: FMC+ Sections A-E.SchDoc | Sheet: 11 of 15 |
| Drawn By: | Contact: http://www.ti.com/support | Size: B |
| Engineer: GBR | | |

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FMC+ Section Rows F - H, J, K

A

B

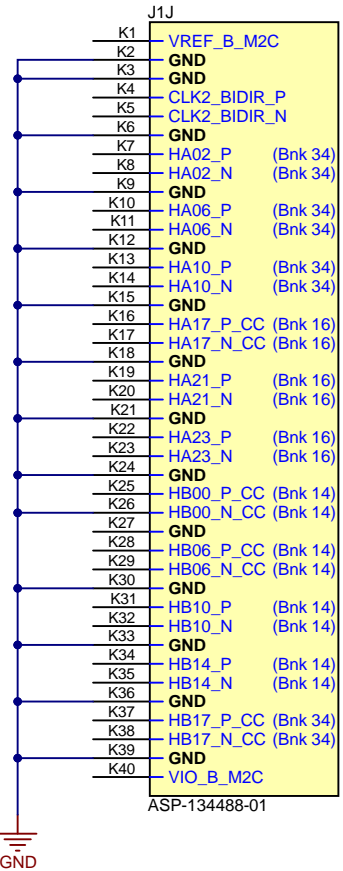
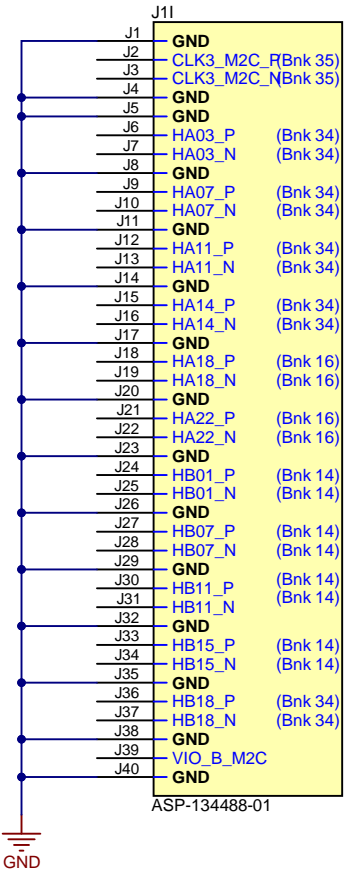
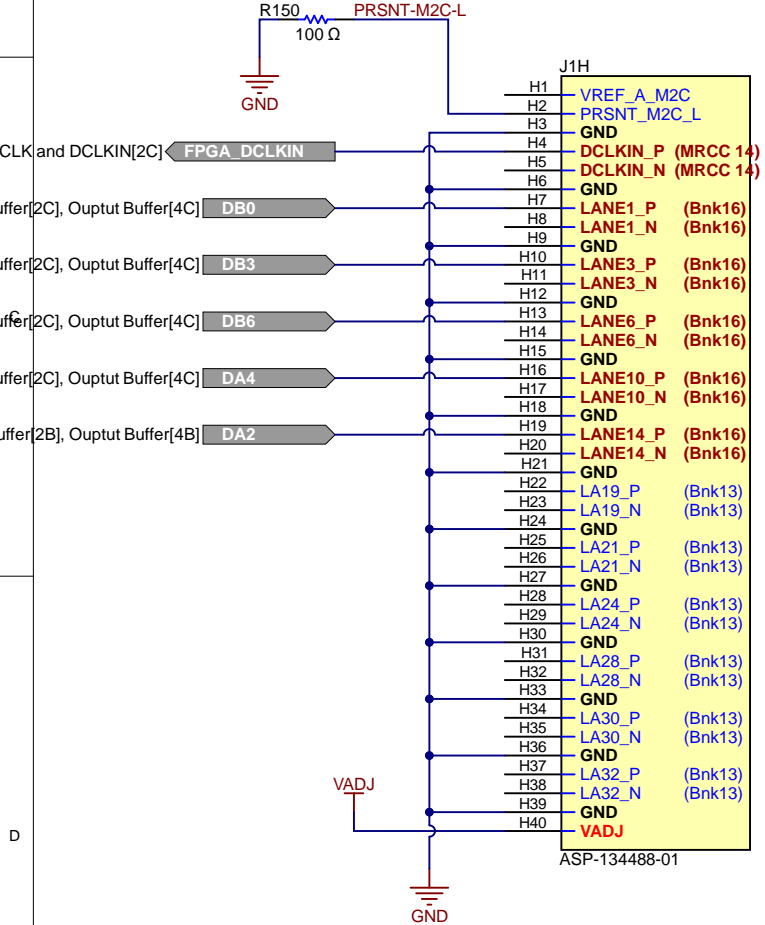
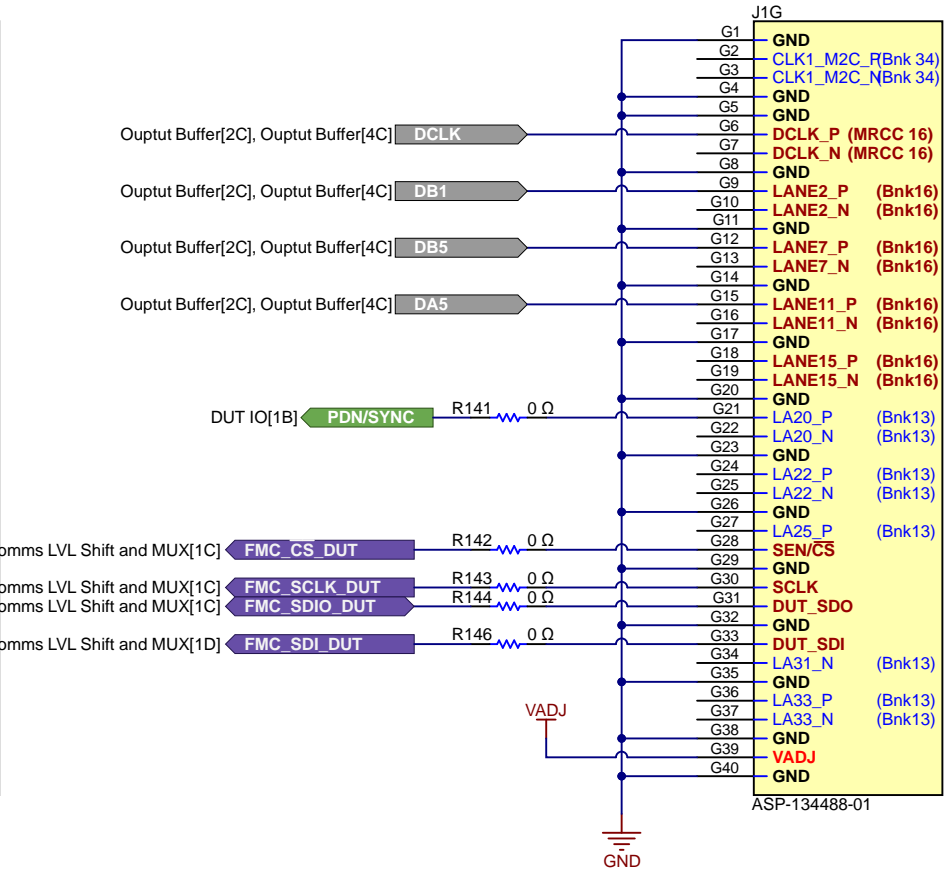
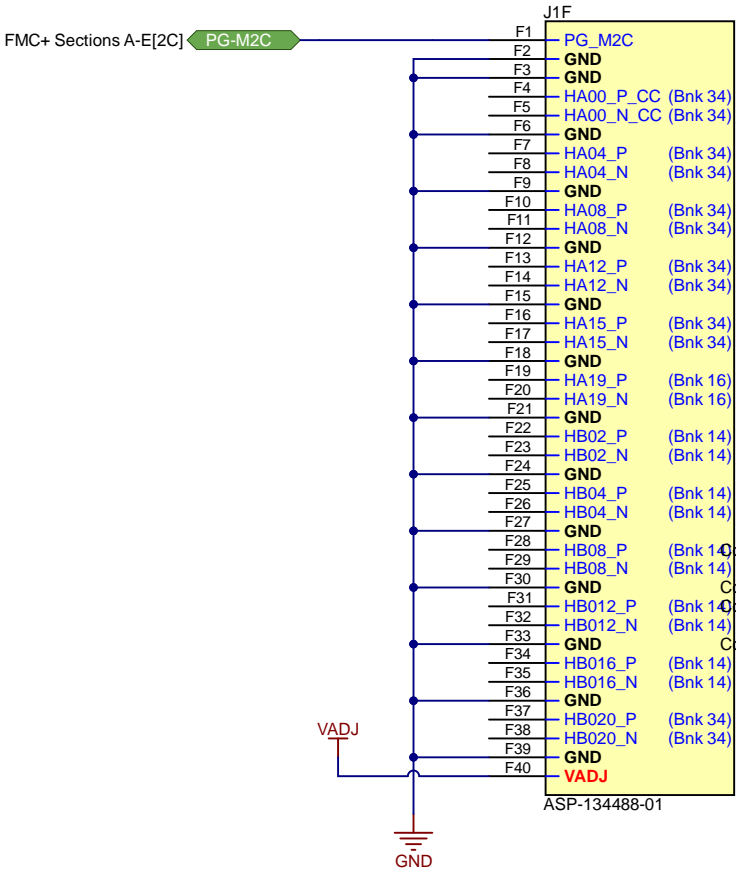
D

A

B

C

D



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|---|--------------------------------------|--|
| Orderable: ChangeMe in variant | Designed for: Public Release | Mod. Date: 8/27/2025 |
| TID #: N/A | Project Title: ADC3644EVM | |
| Number: DC104 | Rev: G2 | Sheet Title: FMC+ Section Rows F - H, J, K |
| SVN Rev: c5e7066f3c60874fd84c3f16880f1305d14003 | ADC3660 | Sheet: 12 of 15 |
| Drawn By: | File: FMC+ Sections F-H, J, K.SchDoc | Size: B |
| Engineer: GBR | Contact: http://www.ti.com/support | |

Output Buffer

A

B

C

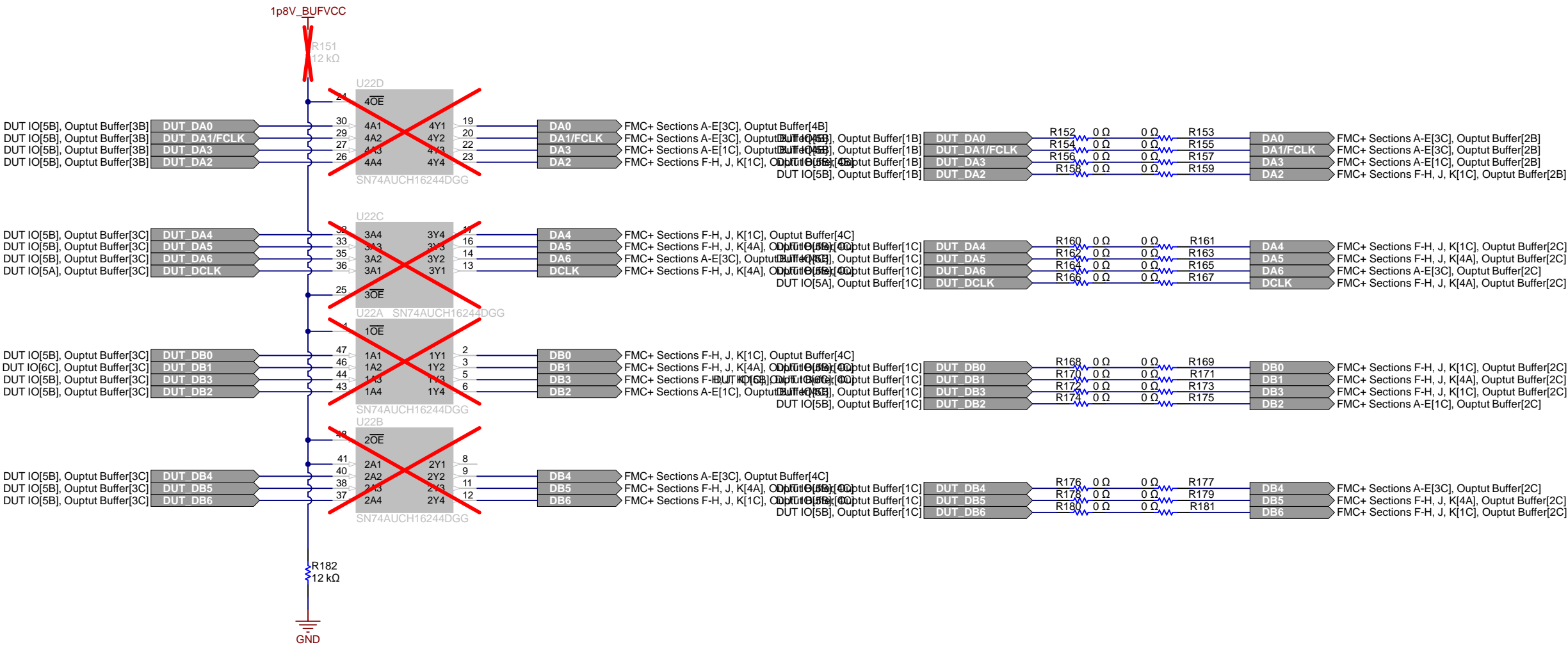
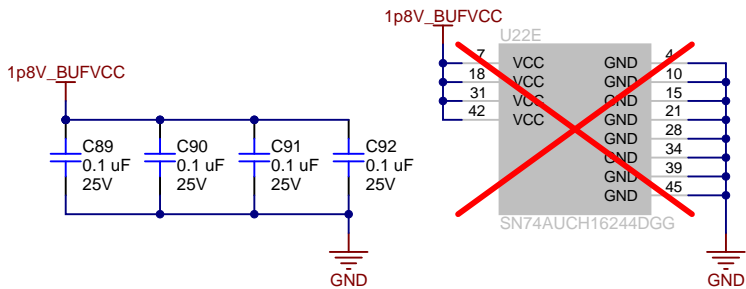
D

A

B

C

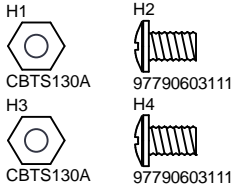
D



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| Orderable: ChangeMe in variant | | Designed for: Public Release | Mod. Date: 8/27/2025 |
| TID #: | N/A | Project Title: ADC3644EVM | |
| Number: DC104 | Rev: G2 | Sheet Title: Output Buffer | |
| SVN Rev: 0758d087f4c4191eb29644a477280b | | Assembled by: 4477280b (ADC3660) | Sheet: 13 of 15 |
| Drawn By: | | File: Ouput Buffer.SchDoc | Size: B |
| Engineer: GBR | | Contact: http://www.ti.com/support | |

Hardware & Mechanicals



PCB Number: DC104

PCB Rev: G2



PCB

LOGO

FCC disclaimer



LBL1

PCB Label

THT-14-423-10

Size: 0.65"x0.20"

ZZ1

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

-

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| | | | |
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| Orderable: ChangeMe in variant | | Designed for: Public Release | Mod. Date: 8/27/2025 |
| TID #: N/A | | Project Title: ADC3644EVM | |
| Number: DC104 | Rev: G2 | Sheet Title: Hardware & Mechanicals | |
| SVN Rev: c5e7066f3c60874fd8f4c346880f30e5d4903 | ADC3660 | | Sheet: 14 of 15 |
| Drawn By: | File: Hardware & Mechanicals.SchDoc | | Size: B |
| Engineer: GBR | Contact: http://www.ti.com/support | | |

Rev History & Variants

Revision History

| Rev | Release Date | Notes |
|-----|--------------|--------------------------|
| G | Feb - 2024 | Complete redesign of EVM |
| | | |
| | | |

Variant(s)

| Variant | Notes |
|---------------|--|
| 001 (ADC3644) | U1: ADC3644 DNI: TP1, TP2, R10, R15, R23, R55, R59, R60, R63, R65, R66, R67, R68, C63, R83, R91, C71, R95, R103, R112, R76, (BUFFER BYPASS), R107, R109 |
| 002 (ADC3643) | U1: ADC3643 DNI: TP1, TP2, R10, R15, R23, R55, R59, R60, R63, R65, R66, R67, R68, C63, R83, R91, C71, R95, R103, R112, R76, (BUFFER BYPASS), R107, R109 |
| 003 (ADC3660) | U1: ADC3660 DNI: TP1, TP2, R10, R15, R23, R55, R59, R60, R63, R65, R66, R67, R68, C63, R83, R91, C71, R95, R103, R112, R76, (BUFFER BYPASS), R108, R109 |

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| | | |
|--|--|---|
| Orderable: ChangeMe in variant | Designed for: Public Release | Mod. Date: 8/27/2025 |
| TID #: N/A | Project Title: ADC3644EVM | |
| Number: DC104 | Rev: G2 | Sheet Title: Rev History & Variants |
| SVN Rev: 5e6878f2674d92c39ae18a4606c9b51470b | Part Number: ADC3660 | Sheet: 15 of 15 |
| Drawn By: | File: Revision History.SchDoc | Size: B |
| Engineer: GBR | Contact: http://www.ti.com/support | |